

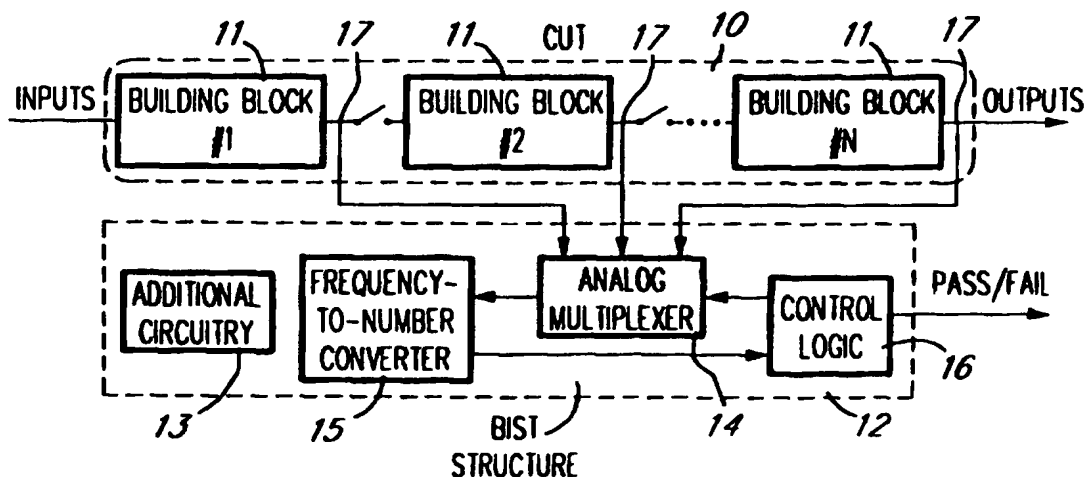
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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : G01R 31/3167, 31/316		A1	(11) International Publication Number: WO 97/15838
			(43) International Publication Date: 1 May 1997 (01.05.97)
(21) International Application Number: PCT/CA96/00701		(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).	
(22) International Filing Date: 22 October 1996 (22.10.96)			
(30) Priority Data: 08/546,806 23 October 1995 (23.10.95) US			
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(54) Title: OSCILLATION-BASED TEST STRATEGY FOR ANALOG AND MIXED-SIGNAL CIRCUITS



(57) Abstract

The oscillation-based test method and device is applied to at least partially analog circuits. The at least partially analog circuit is first divided into building blocks each having a given structure. Each building block is then inserted into an oscillator circuit to produce an output signal having an oscillation frequency related to the structure of the building block under test. The oscillation frequency is then measured and a fault in the building block under test is detected when the measured oscillation frequency deviates from a given, nominal frequency. Experiments have demonstrated that the frequency deviation enables the detection of catastrophic and/or parametric faults, and ensures a high fault coverage. In this new time-domain test method, a single output frequency is evaluated for each building block whereby the test duration is very short. These characteristics make the test strategy very attractive for wafer-probe testing as well as final production testing.

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5 OSCILLATION-BASED TEST STRATEGY FOR

 ANALOG AND MIXED-SIGNAL CIRCUITS

10

BACKGROUND OF THE INVENTION

15 1. Field of the invention:

 The present invention relates to a method
 and device for testing analog and mixed-signal
 circuits.

20

 In the present disclosure and in the
 appended claims, the term "mixed signal circuit" is
 intended to designate a circuit including both analog
 and digital circuitry.

25

2. Brief description of the prior art:

 Due to the development of integrating
 technologies and the market requirements, the trend of
30 designing mixed-signal ASICs (Application-Specific
 Integrated Circuits) has significantly increased.

5 Analog testing is a challenging task and is considered
as one of the most important problems in analog and
mixed-signal ASIC design. The specifications of
analog circuits are usually very large which results
in long testing time and poor fault coverage. A
10 dedicated test equipment is also required.
Furthermore, it is very difficult to establish
universal fault models equivalent to the so called
stuck-at models in digital circuits.

15 A fault can be either catastrophic or
parametric. Catastrophic faults result in complete
absence of the desired function. On the other hand,
parametric faults result in functional circuit but
with degraded performance. Catastrophic faults are
20 easier to test, but when the complexity of the CUT
(Circuit Under Test) increases they cause many
problems. Parametric faults are the most important
and hard to test faults. It should be pointed out
that most of the existing test methods address only
25 the catastrophic faults.

Known methods for testing analog blocks
comprise functional (or parametric) testing, DC
(Direct Current) testing, and power supply current
30 (I_{DDQ}) monitoring. Functional (or parametric) testing
has been described in the following four articles:

- 5 [1] C.-L Wey, "Built-In Self-Test Structure
for Analog Circuit Fault Diagnosis", *IEEE
Transactions on Instrumentation and
Measurement*, 39(3), 1990, pp. 517-521.
- 10 [2] L. Milor et al., "Optimal Test Set Design
for Analog Circuits", *IEEE ICCAD*, 1990,
pp. 294-297.
- 15 [3] P.P. Fasang, D. Mulins and T. Wong,
"Design for Testability for Mixed
Analog/Digital ASICs", *IEEE Custom
Integrated Circuit Conf.*, 1988, pp.
16.5.1-16.5.4.
- 20 [4] K.D. Wagner and T.W. Williams, "Design
for Testability of Mixed signal
Integrated Circuits", *IEEE Int. Test
Conf.*, 1988, pp.823-829.
- 25 DC testing has been suggested in the following two
articles:
- 30 [5] M.J. Marlett and J.A. Abraham, "DC IATP-
An Iterative Analog Circuit Test
Generation Program for Generating Single

5 Pattern Tests", IEEE Int. Test Conf.,
1988, pp. 839-844.

[6] G. Devarayanadurg and M. Soma,
"Analytical Fault Modelling and Static
10 Test Generation for Analog ICs", *IEEE*
ICCAD, 1994, pp.44-47.

Power-supply current (I_{DDQ}) monitoring is discussed in the following two publications:

15 [7] G. Gielen, Z. Wang and W. Sansen, "Fault
Detection and Input Stimulus
Determination for the Testing of Analog
Integrated Circuits Based on Power-Supply
20 Current Monitoring", *IEEE ICCAD*, 1994,
pp.495-498.

[8] P. Nigh and W. Maly, "Test Generation for Current Testing", IEEE Design & Test of Computers, Vol. 7, No. 2, 1990, pp.26-38.

Various designs for testability (DFT) rules have been used in conjunction with the above mentioned test methods to ease the test problem (articles [3] and [4]). These techniques are employed during the design stage to increase the

5 controllability and observability and to facilitate
the test task. Some of these techniques for digital
testing have been the subject of US patent No.
4,513,418 (P.H. Bardell et al.) issued on April 23,
1985 for an invention entitled "Simultaneous Self
10 Testing System" and US patent No. 4,749,947 granted to
T.R. Gheewala on June 7, 1988 for an invention
entitled "Cross-Check Test Structure for Testing
Integrated Circuits".

15 The effectiveness of the above methods
depends strongly on the selection of suitable test
vectors. Also, they need a large number of test
vectors to validly testing the functionality of the
CUT. When the complexity of the CUT increases, the
20 problem of determining optimal test vectors becomes
critical. Furthermore, the process of choosing a
suitable form of excitation signals and evaluation of
the results is time consuming. BIST (Built-In Self-
Test) strategies based of above methods require the
25 use of specialized input stimuli generation and output
evaluation hardware which introduce significant area
overhead.

5 OBJECTS OF THE INVENTION

 An object of the present invention is
 therefore to overcome the above discussed drawbacks of
10 the prior art.

 Another object of the present invention is
 to overcome the above discussed drawbacks of the prior
 art by providing a very efficient method and device
15 for testing analog and mixed-signal circuits, in which
 the CUT is rearranged into a circuit easier to test.

 A further object of the present invention
 is to provide a method and device for testing analog
20 and mixed-signal circuits, in which the CUT is
 inserted into an oscillation circuit.

SUMMARY OF THE INVENTION

25

 More particularly, in accordance with the
 present invention, there is provided an oscillation-
 based test method for testing an at least partially
30 analog circuit, comprising the steps of:

5 dividing the at least partially analog
circuit into building blocks each having a given
structure;

 inserting each building block under test
into an oscillator circuit to produce an output signal
10 having an oscillation frequency related to the
structure of the building block under test;

 measuring the oscillation frequency of the
output signal; and

 detecting a fault in the building block
15 under test when the measured oscillation frequency
deviates from a given, nominal frequency.

 By inserting the building block under test
into an oscillator circuit producing an output signal
20 having an oscillation frequency related to the
structure of the building block, a catastrophic or
parametric fault in the building block can be easily
detected by simply sensing a deviation of the
measured oscillation frequency from the above
25 mentioned given, nominal frequency.

 In accordance with preferred embodiments
of the oscillation-based test method of the invention:

30 - the measuring step comprises converting the
oscillation frequency of the output signal into a

5 frequency representative number, and the fault
detecting step comprises (a) comparing the frequency
representative number to a given, nominal number, and
(c) detecting a fault in the building block under test
when the frequency representative number deviates from
10 the given, nominal number; and

- the inserting step comprises combining at least two
building blocks to form the oscillator circuit.

15 The present invention is also concerned
with a device for testing an at least partially analog
circuit divided into building blocks each having a
given structure and inserted into an oscillator
circuit to produce an output signal having an
20 oscillation frequency related to the structure of the
building block, comprising:

means for measuring the oscillation
frequency of the output signal; and

means for detecting a fault in the
25 building block under test when the measured
oscillation frequency deviates from a given, nominal
frequency.

In accordance with preferred embodiments
30 of the device according to the invention:

- 5 - the measuring means comprises a frequency-to-number converter for converting the oscillation frequency of the output signal into a frequency representative number, and the fault detecting means comprises a control logic for comparing the frequency
10 representative number to a given, nominal number and for detecting a fault in the building block under test when the frequency representative number deviates from the given, nominal number;
- 15 - the frequency-to-number converter comprises a zero crossing detector for detecting passages of the output signal by a zero amplitude to produce a square wave clock signal including a series of pulses, and a counter for counting the pulses of the square wave
20 clock signal to produce the frequency representative number;
- 25 - the test device further comprises an additional circuitry, and means for connecting the additional circuitry to the building block under test to form an oscillator circuit, wherein these connecting means comprises means for successively connecting the additional circuitry to different building blocks in order to test the different buildings blocks with the
30 same additional circuitry.

5 The objects, advantages and other features
of the present invention will become more apparent
upon reading of the following non restrictive
description of preferred embodiments thereof, given by
way of example only with reference to the accompanying
10 drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

15

In the appended drawings:

Figure 1 is a schematic block diagram
illustrating an oscillation-based built-in self test
20 (OBIST) embodying the test method of the present
invention, for analog and mixed-signal circuits;

Figure 2 is a schematic block diagram of
a frequency-to-number converter used in the
25 oscillation-based test method of Figure 1;

Figure 3 is a schematic block diagram
illustrating an embodiment of the oscillation-based
test method in accordance with the present invention,
30 to improve the testability of analog and mixed-signal
circuits;

5 Figure 4a is a schematic block diagram illustrating a first mathematical approach for inserting a CUT into an oscillator circuit using a negative feedback loop;

10 Figure 4b is a schematic block diagram illustrating a second mathematical approach for inserting a CUT into an oscillator circuit using a positive feedback loop;

15 Figure 5 is a schematic block diagram showing a DFT technique for inserting an operational amplifier (CUT) into an oscillator circuit in which the oscillation frequency is related to the internal structure of the operational amplifier;

20 Figure 6 is a schematic block diagram showing a DFT technique for inserting two operational amplifiers (CUT) into an oscillator circuit whose oscillation frequency depends on the internal
25 structure of the two operational amplifiers under test;

 Figure 7 is a schematic block diagram showing a DFT technique for inserting a chain of
30 operational amplifiers (CUT) into an oscillator circuit;

5 Figure 8 is a schematic block diagram showing a DFT technique for inserting a high-Q band-pass filter into an oscillator circuit by means of a positive feedback loop including a zero-crossing detector;

10

 Figure 9 is a diagram showing the implementation of the method of Figure 8 to a second order active band-pass filter;

15

 Figure 10 is a schematic block diagram of a dual-slope analog-to-digital converter; and

 Figure 11 is a schematic block diagram of an oscillation-based test structure for inserting the analog port of the dual-slope analog-to-digital converter of Figure 10 into an oscillator circuit.

20

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

25

 The following description will show how the oscillation-based testing method in accordance with the present invention can be applied to common integrated analog or mixed-signals circuits such as embedded operational amplifiers, filters, and analog-

30

5 to-digital converters. However, it should be kept in mind that the method and device in accordance with the present invention can be easily applied to other types of circuits such as functional analog circuits and non integrated circuits.

10

More specifically, Figure 1 illustrates a basic BIST structure suitable for use in the oscillation-based testing method according to the invention.

15

Referring to Figure 1, the method first comprises the step of dividing the CUT 10 into building blocks such as 11. The CUT is then in the test mode.

20

The BIST structure 12 comprises some additional circuitry 13 integrated to the CUT 10 and to be connected to each building block 11 to form with this building block 11 an oscillator circuit producing
25 an output signal having an oscillation frequency related to the structure of the building block 11 under test. Examples of additional circuitry 13 suitable to form with the building blocks 11 oscillator circuits will be described in the following
30 description.

5 The BIST structure 12 of Figure 1 further
comprises an analog multiplexer 14, a frequency-to-
number converter 15, and a control logic 16. The
analog multiplexer 14 is connected to the different
10 outputs 17 of the building blocks 11 to successively
select these outputs 17 under the control of the
control logic 16. The oscillation frequency of the
signal at the output 17 of the building block 11 being
selected by the analog multiplexer 14 is converted to
15 a frequency representative number by the frequency-to-
number converter 15. The control logic 16 then
compares the frequency representative number from the
frequency-to-number converter 15 to a given, nominal
number corresponding a nominal frequency of
oscillation of the so formed oscillator circuit, and
20 detects a fault in the building block 11 under test
when the frequency representative number deviates the
given, nominal number. When the frequency
representative number corresponds to the given,
nominal number, the control logic 16 delivers a "pass"
25 signal indicating that the building block 11 under
test is fully functional. On the contrary, when the
frequency representative number from the converter 15
deviates from the given, nominal number, the control
logic 16 delivers a "fail" signal indicating that the
30 building block 11 of the CUT 10 is faulty.

5 To verify the functionality of the BIST structure 12 itself, the circuitry of the BIST structure 12 is tested during a self-test phase before testing the CUT 10.

10 Figure 2 is a schematic block diagram of the frequency-to-number converter 15 of Figure 1.

 The frequency-to-number converter 15 can be implemented using various techniques such as a
15 phase-locked loop (PLL) or any type of FM (Frequency Modulation) demodulator. The preferred embodiment of Figure 2 uses a simple and fully digital circuit capable of converting each frequency to a related number. The oscillation frequency f_{osc} of the selected
20 output 17 is supplied by the analog multiplexer 14 to a zero crossing detector 19. The zero crossing detector 19 detects passages of the oscillation output signal by a zero amplitude to produce on its output 20 a square wave clock signal including a series of
25 pulses and applied to a counter 21. The counter 21 is enabled by the high signal level of a square wave reference frequency f_{ref} . Therefore, during the high signal level of the square wave reference frequency f_{ref} , the counter 21 counts the pulses from the output
30 20 while during its low signal level the counter 21 is disabled and stops counting. The counter 21 delivers

5 an output digital count value on a parallel output 22.
The output count value from the parallel output 22 of
the counter 21 is representative of a number related
to the input frequency f_{osc} coming from the output 17
of a building block 11 under test, and can be
10 evaluated by the control logic 16. After evaluation
of the output frequency representative number from the
counter 21, the control logic 16 resets the counter 21
through the input 23 thereof. Those of ordinary skill
in the art will appreciate that an accurate frequency-
15 to-number conversion is obtained; the accuracy of the
frequency-to-number converter 15 is determined by the
reference frequency f_{REF} signal and the number of bits
of the parallel output 22 of the counter 21. More
specifically, the digital output of the counter 21 is
20 given by the following relation:

$$B_{1:n} \propto \frac{(f_{OSC}/f_{REF})}{2}$$

In fact, the oscillation frequency f_{osc} is
divided by the reference frequency f_{REF} to obtain the
25 number $B_{1:n}$. This technique produces a very good
accuracy and satisfies the requirement of the intended
application.

5 In the example of Figure 3, the oscillation-based test method is used to facilitate the test problem. The test structure 12 then comprises the additional circuitry 13, the analog multiplexer 14 and the control logic 16.

10

 Again, the additional circuitry 13 is to be connected to each building block 11 to form with this building block 11 an oscillator circuit producing an output signal having an oscillation frequency related to the structure of the building block 11 under test. The analog multiplexer 14 is connected to the different outputs 17 of the building blocks 11 to successively select these outputs 17 under the control of the logic 16. The oscillation frequency f_{osc} at the output 17 of the building block 11 being selected by the analog multiplexer 14 is then supplied to an output 18 of the test structure 12. The oscillation frequency f_{osc} from the output 18 of the BIST structure 12 is evaluated externally using a test equipment (not shown). The embodiment of Figure 3 enables an important simplification of the control logic 16 and more generally of the test structure 12. In this case, since the oscillation frequency is externally evaluated, the voltage level of the oscillation frequency signal from the output 17 of the building

15

20

25

30

5 block 11 being tested can also be evaluated to improve
the fault coverage.

For each type of building block 11,
various techniques can be easily found to insert the
10 building block into an oscillator circuit. A
mathematical approach is to convert the transfer
function of the CUT to the transfer function of an
oscillator, and then to modify the internal circuitry
of the CUT to obtain the new transfer function. For
15 example, second order active filters can be converted
to oscillators by making the quality factor Q_F
infinite, which means that the poles are on the $j\omega$
axis. A more general technique consists of performing
some mathematical operations to obtain the
20 oscillator's transfer function.

In the example of Figure 4a, a negative
feedback loop 24 including a transfer function F_H and
and adder 25 is added to the transfer function F_{CUT} of
25 the building block 11 to achieve the transfer function
 F_{OSC} of an oscillator. The transfer function F_{OSC} of
Figure 4a can then be expressed as follows:

$$F_{osc} = \frac{F_{cut}}{(1 + F_{cut} F_H)}$$

5

Thus F_H is given by the following relation:

$$F_H = \frac{(F_{cut} - F_{osc})}{(F_{cut} F_{osc})}$$

Another approach is illustrated in Figure
 10 4b. The approach of Figure 4b consists of adding to
 the transfer function F_{cut} of the building block 11 a
 positive feedback loop 26 including a transfer
 function F_H and an adder 27, and of trying to satisfy
 the condition of oscillation by appropriately
 15 selecting the parameters of the transfer function F_H .
 In that case, the new transfer function is given by
 the following relation:

$$F_{osc} = \frac{F_{cut}}{(1 - F_{cut} F_H)}$$

and the condition for the feedback loop to cause
 20 sinusoidal oscillations of frequency ω_o is that:

$$|F_{cut}(j\omega_o)| |F_H(j\omega_o)| \geq 1$$

5 and the phase of the signal ϕ around the loop is such that:

$$\phi_A + \phi_B = 0^\circ$$

where ϕ_A and ϕ_B are the phase shifts associated with the CUT and feedback network, respectively.

10

It is further possible to add both positive and negative feedback loops and then to force the resulting circuit to oscillate.

15

A further possible solution is to employ heuristic circuit techniques to obtain an oscillator from the original building block 11 of the CUT.

20

Some examples of application of the oscillation-based test method in accordance with the present invention will now be described. These examples are given for the purpose of exemplification only and should not be interpreted as limiting the scope of the invention.

25

5 **Figure 5**

 The operational amplifiers are the blocks most frequently encountered in analog and mixed-signal
10 circuits. For analog functional blocks with embedded operational amplifiers, the test procedure will be easier and the fault coverage will be higher if it can be assumed that the operational amplifiers are not faulty. Therefore, the interest of developing an
15 efficient technique to test operational amplifiers is obvious.

 In Figure 5, an operational amplifier 28 is tested. To perform the test, the operational
20 amplifier 28 is inserted into a simple operational-amplifier-based oscillator circuit 29. In this particular case, the additional circuitry 13 comprises two transistors 30 and 31, a resistor 32 and a capacitor 33, forming part of the integrated circuit
25 and connectable as shown in Figure 5 to the operational amplifier 28 through switching elements 34-36 for the duration of the test. After the test, the switching elements are opened to disconnect the operational amplifier 28 from the additional circuitry
30 13. The switching elements 34-36 are semiconductor elements such as transistors or the like which, in the

5 closed state of the switching elements 34-36 have a low resistance to minimize performance degradation. The area overhead due to these switching elements 34-36 on the integrated circuit (CUT) being tested is very, very small.

10

The oscillation frequency of the circuit of Figure 5 depends on the value of the internal dominant pole and the DC open loop gain of the operational amplifier 28, the resistance R of the resistor 32, and the capacitance C of the capacitor 33. The transistors 30 and 31 are used as active resistors to introduce a positive feedback and are adjusted to guarantee a sustained oscillation.

20

The additional circuitry 13 is used for all the operational amplifiers of the chip (CUT 10) whereby the area overhead is very small. The operational amplifiers are successively connected to, that is inserted in the oscillator circuitry of Figure 5 through the above mentioned switching elements and, as described in the foregoing description, the oscillation frequency is evaluated to determine whether the operational amplifier is faulty or not.

25

5 Simulations have shown that the majority
of catastrophic faults result in a loss of
oscillation.

Figure 6

10

 Another oscillator circuit 36 suitable for
simultaneously testing two operational amplifiers 37
and 38 is illustrated in Figure 6 and has been
described in the article of R. Senani entitled "Simple
15 Sinusoidal Oscillator Using Opamp Compensation Poles",
published in *Electronic Letters*, Vol.29, No. 5, 1993,
pp. 452-453. The oscillator circuit 36 of Figure 6 is
a simple sinusoidal oscillator using the compensation
poles of the operational amplifiers 37 and 38 and,
20 therefore, the oscillation frequency is tightly
related to the internal structure of these operational
amplifiers 37 and 38. The additional circuitry 13
simply comprises a resistor 39 and a capacitor 40
whereby the area overhead on the integrated circuit is
25 smaller than in the previous circuit illustrated in
Figure 5. The connections between the operational
amplifiers 37 and 38, the resistor 39 and the
capacitor 40 are clearly shown in Figure 6 and can be
established through switching elements (not shown) as
30 described with reference to Figure 5 for the duration

5 of the test. The condition of oscillation and the frequency of oscillation f_{osc} are

$$(\omega_{t1} - \frac{1}{\tau}) \leq 0$$

and

$$f_{osc} = \sqrt{(f_{t1} f_{t2})}$$

respectively, where ω_{t1} is the GBW (unity-gain bandwidth) of the first operational amplifier 37, $\tau =$
10 RC and $f_{t1} = \omega_{t1}/2\pi$.

Experiments with the oscillators of Figures 5 and 6 have proved that both catastrophic and parametric faults manifest as a deviation of the
15 oscillation frequency from the given, nominal frequency and, therefore, can be easily detected.

Figure 7

20 An approach to speed up the test process is to place all the operational amplifiers 46 of a given CUT into a chain to construct an oscillator circuit 41 as illustrated in Figure 7. The additional
circuitry 13 then simply comprises two transistors 42
25 and 43, a resistor 44, and a capacitor 45

5 interconnected with the chain of operational
amplifiers 46 as illustrated in Figure 7. With the
circuit of Figure 7, the test time is significantly
reduced but the fault coverage will be smaller.
However, a hard fault in any of the operational
10 amplifiers 46 deviates the oscillation frequency from
its nominal value and, therefore, is detectable.

Figure 8

15 In this example, a high-Q band-pass filter
47 is converted to an oscillator using a quite simple
technique. The basic principle of the example of
Figure 8 is to place the band-pass filter 47 in a
positive-feedback loop 50 including a zero-crossing
20 detector 48 or a hard limiter. The wide band noise at
the input 49 of the band-pass filter 47 is filtered
and only a sine wave signal whose frequency is equal
to the center frequency of the filter is passed. The
zero-crossing detector 48 delivers on its output 51 a
25 square wave whose frequency is ω_0 . This square wave is
applied to the input 49 of the band-pass filter 47 and
this filter 47 generates a sine wave at the
fundamental frequency ω_0 . The zero-crossing detector
48 introduces a very high gain to guarantee a
30 sustained oscillation. Again, the zero-crossing
detector 48 can be connected to the band-pass filter

5 47 through switching elements 52 and 53 for the duration of the test.

Figure 9

10 This figure shows the implementation of the method of Figure 8 for a second order active band-pass filter which has a center frequency of approximately 25 kHz.

15 Experimentation of the circuits of Figures 8 and 9 have demonstrated that both catastrophic and parametric faults can be detected.

20 To enable the use of the method of Figures 8 and 9, other filter circuits can be converted to a band-pass filter using mathematical transformations as explained earlier for the conversion of a given circuit to an oscillator. Also, the output of a low-pass and high-pass filter may be added together to
25 obtain a band-pass output. The input of a notch filter may be subtracted from its output to construct a band-pass filter. State variable filters can be tested using their band-pass output. It should also be noted that other techniques are available to
30 construct an oscillator from a filter.

5 Figures 10 and 11

Figure 10 illustrates a dual-slope analog-to-digital converter 53. The analog part of the converter 53 comprises an integrator 54 and a
10 comparator 55. The integrator 54 comprises an operational amplifier 56, a resistor 57 having a resistance R, and a capacitor 58 having a capacitance C. The comparator 55 comprises an operational amplifier 59. The property of integrating the input
15 signal 63 by means of the integrator 54 makes the converter 53 immune to noise. The converter 53 further comprises a control logic 60 controlling an input switch 61 through which the input analog signal 63 is supplied to one terminal of the resistor 57, and
20 serving as an interface between the output of the operational amplifier 59 and an output register 62 producing the digital version 64 of the input signal 63. The different components of the analog-to-digital converter 53 are interconnected as shown in Figure 10.
25 The structure of the analog-to-digital converter 53 is well known to those of ordinary skill in the art and accordingly will not be further described.

Figure 11 presents a test solution for the
30 analog-to-digital converter of Figure 10, based on the test method in accordance with the present invention.

5 At the first test phase, the existing integrator 54 and comparator 55 are rearranged to a multivibrator using additional resistors R_a and R_b , and switching elements 65 and 66 controllable through the control logic 60. The different components are interconnected
10 as illustrated in Figure 11. The oscillation frequency and the oscillation condition of the multivibrator circuit of Figure 11 are respectively given by the following relations:

$$f_{osc} = \frac{1}{4RC} \left(\frac{R_b}{R_a} \right)$$

and

$$R_b > R_a$$

15 The above equation assumes that the operational amplifiers are ideal and does not express the effect of the internal characteristics of these operational amplifiers. These effects can be neglected when the operational amplifiers are fault-free, but when there
20 is a fault in the operational amplifiers they influence the oscillation frequency.

The oscillation frequency f_{osc} is converted to a number by the existing counter (output register
25 62). The obtained number is compared with the given,

5 nominal number to verify whether there is a fault in
the structure of the analog-to-digital converter 53.

At the second test phase, the analog-to-digital converter 53 is rearranged into a functional
10 mode in which a voltage reference $-V_{REF}$ is supplied to
the integrator 54 through the switch 61, and converted
to digital. The digital number obtained is compared
with a second, given test signature number to verify
the functionality of the digital part of the analog-
15 to-digital converter 53 and also of value of the
signal $-V_{REF}$. The operation is directed by the control
logic. All the internal blocks of the analog-to-
digital converter 53 contribute to the test structure
and are therefore tested in a single operation. The
20 simplicity and efficiency of the test architecture of
Figure 11 is obvious. Oversampled analog-to-digital
converters have analog components similar to those of
Figure 10; therefore, the same test technique can be
applied to them.

25

The example of Figures 10 and 11 proposes
an approach which consists of combining different
building blocks such as Schmitt triggers, comparators,
integrators and amplifiers to construct an oscillator
30 and thereby enable testing in accordance with the
present invention.

5 Other types of building blocks can also be
placed in an oscillator using circuit techniques which
are well known to those of ordinary skill in the art
of integrated oscillators. Since proposing all the
circuit techniques available to convert building
10 blocks to an oscillator is not the main objective of
the invention, the present disclosure will be limited
to the examples of Figures 4a, 4b, and 5-11 which are
believed to be sufficient to allow integrated circuit
designers to achieve the technique and assure the
15 testability of analog circuits.

 Although the present invention has been
applied to some specific electronic circuits and some
preferred embodiments thereof have been described, it
20 should be understood that many modifications and
changes may be made in the illustrated embodiments
without departing from the spirit and scope of the
invention and that the method is not limited to the
presented building blocks.

WHAT IS CLAIMED IS:

1. An oscillation-based test method for testing an at least partially analog circuit, comprising the steps of:

dividing said at least partially analog circuit into building blocks each having a given structure;

inserting each building block under test into an oscillator circuit to produce an output signal having an oscillation frequency related to the structure of the building block under test;

measuring the oscillation frequency of said output signal; and

detecting a fault in the building block under test when the measured oscillation frequency deviates from a given, nominal frequency.

2. An oscillation-based test method as recited in claim 1, wherein said fault detecting step comprises detecting catastrophic and/or parametric faults in response to a deviation of the measured oscillation frequency from said given, nominal frequency.

3. An oscillation-based test method as recited in claim 1, wherein said measuring step comprises the step of converting the oscillation

frequency of said output signal into a frequency representative number.

4. An oscillation-based test method as recited in claim 3, wherein said fault detecting step comprises the steps of:

comparing the frequency representative number to a given, nominal number; and

detecting a fault in the building block under test when the frequency representative number deviates from said given, nominal number.

5. An oscillation-based test method as recited in claim 3, wherein said converting step comprises the steps of:

detecting passages of said output signal by a zero amplitude to produce a square wave clock signal including a series of pulses; and

counting the pulses of said square wave clock signal to produce the frequency representative number.

6. An oscillation-based test method as recited in claim 1, wherein said inserting step comprises the step of combining at least two of said building blocks to form said oscillator circuit.

7. An oscillation-based test method as recited in claim 1, wherein said at least partially

analog circuit is an integrated circuit, and wherein said step of inserting each building block under test into an oscillator circuit comprises the steps of:

integrating an additional circuitry into said integrated circuit; and

connecting said additional circuitry to the building block under test to form said oscillator circuit.

8. An oscillation-based test method as recited in claim 7, wherein said connecting step comprises the step of connecting said additional circuitry to the building block under test through switching elements, and wherein said oscillation-based test method further comprises the step of opening said switching elements to disconnect said additional circuitry from the building block under test when said fault detecting step is completed.

9. An oscillation-based test method as recited in claim 1, wherein said fault detecting step comprises producing a fail signal when the measured oscillation frequency deviates from said given, nominal frequency, and producing a pass signal when the measured oscillation frequency corresponds to said given, nominal frequency.

10. A device for testing an at least partially analog circuit divided into building blocks

each having a given structure and inserted into an oscillator circuit to produce an output signal having an oscillation frequency related to the structure of the building block, comprising:

means for measuring the oscillation frequency of said output signal; and

means for detecting a fault in the building block under test when the measured oscillation frequency deviates from a given, nominal frequency.

11. The device of claim 10, wherein said fault detecting means comprises means for detecting catastrophic and/or parametric faults in response to a deviation of the measured oscillation frequency from said given, nominal frequency.

12. The device of claim 10, wherein said measuring means comprises a frequency-to-number converter for converting the oscillation frequency of said output signal into a frequency representative number, and wherein said fault detecting means comprises a control logic for comparing the frequency representative number to a given, nominal number and for detecting a fault in the building block under test when the frequency representative number deviates from said given, nominal number.

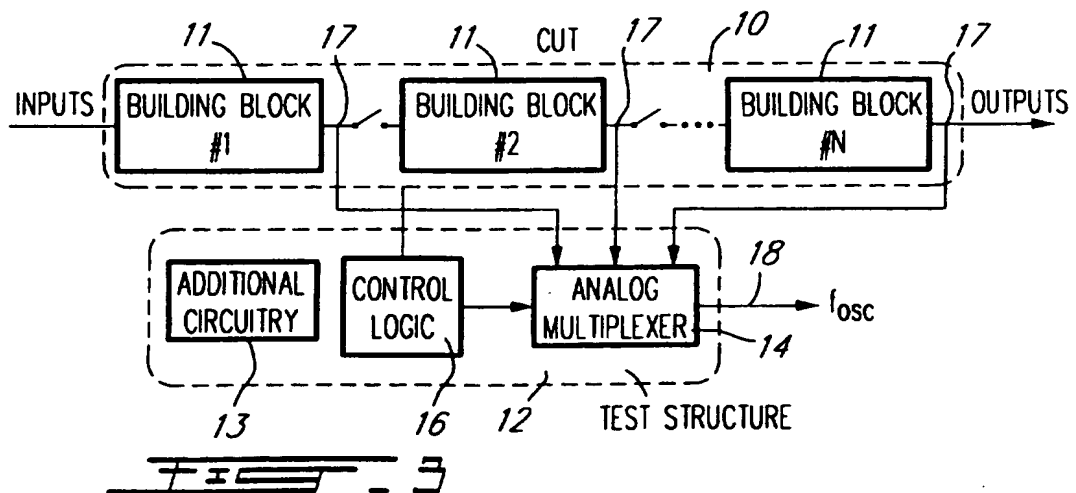
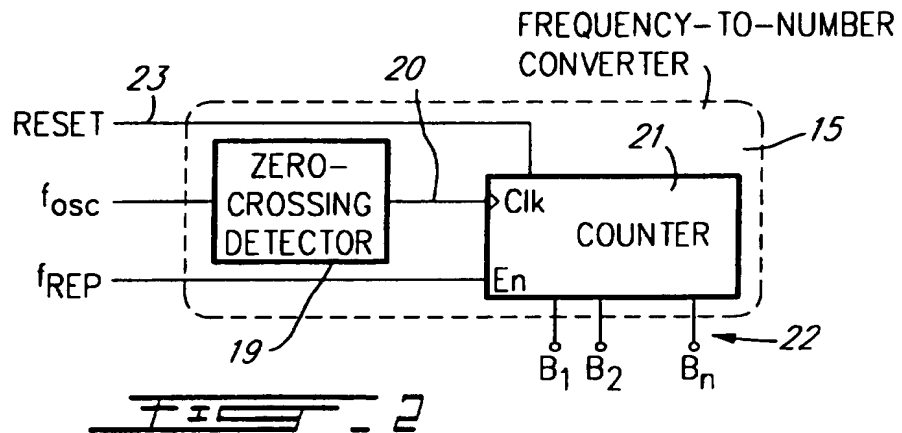
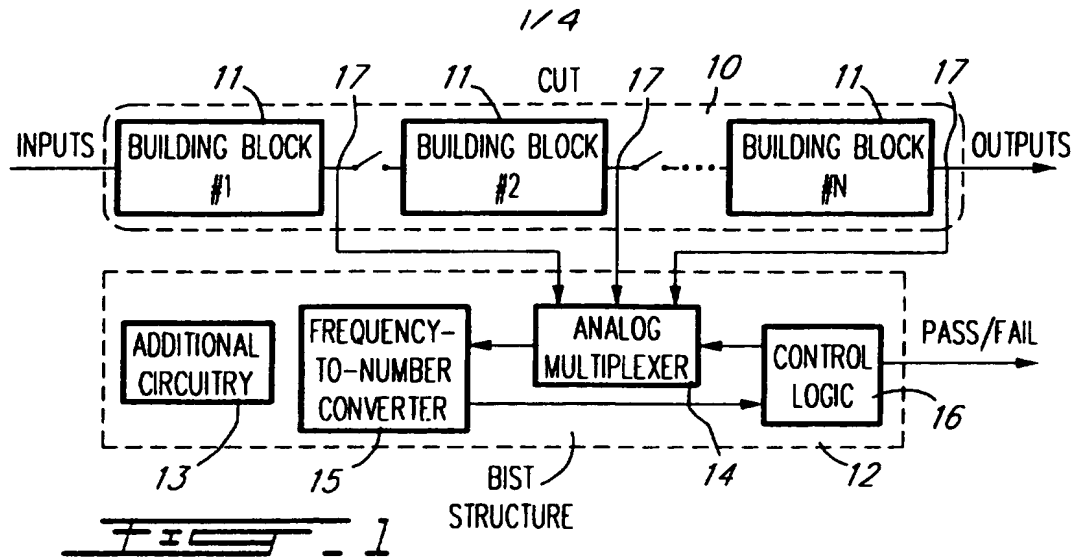
13. The device of claim 12, wherein said frequency-to-number converter comprises a zero crossing detector for detecting passages of said output signal by a zero amplitude to produce a square wave clock signal including a series of pulses, and a counter for counting the pulses of said square wave clock signal to produce the frequency representative number.

14. The device of claim 10, wherein said fault detecting means comprises a control logic for producing a fail signal when the measured oscillation frequency deviates from said given, nominal frequency, and for producing a pass signal when the measured oscillation frequency corresponds to said given, nominal frequency.

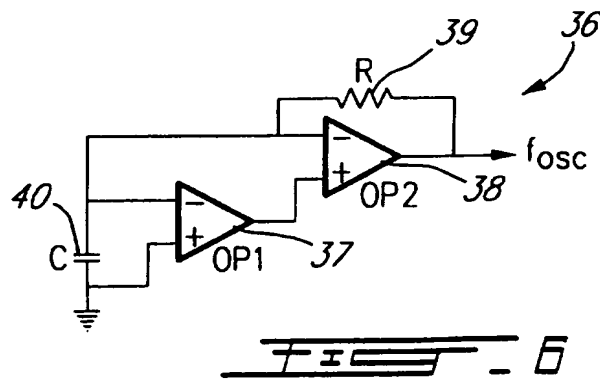
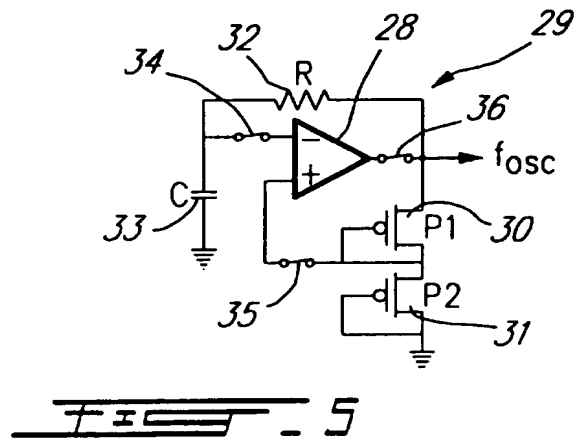
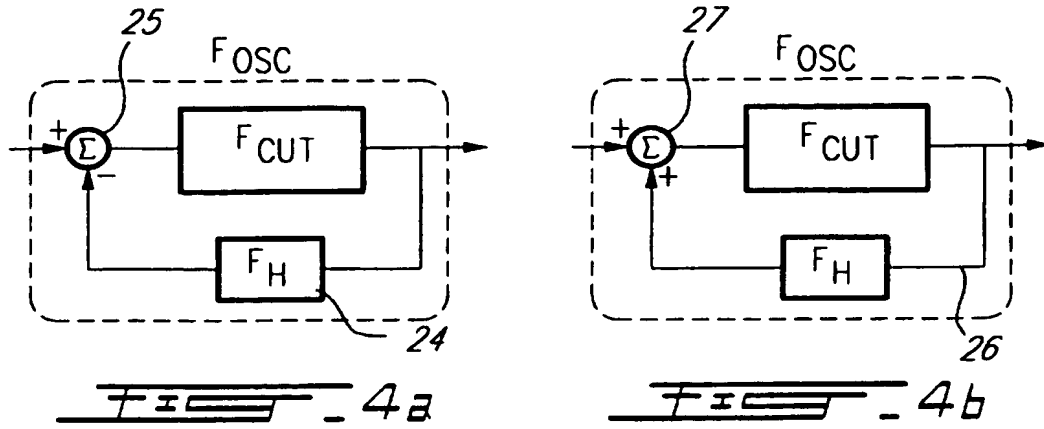
15. The device of claim 10, further comprising:

an additional circuitry; and
means for connecting said additional circuitry to the building block under test to form an oscillator circuit.

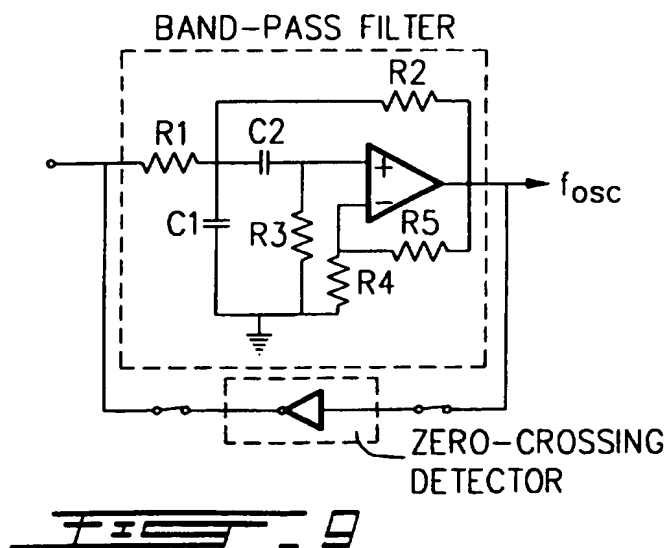
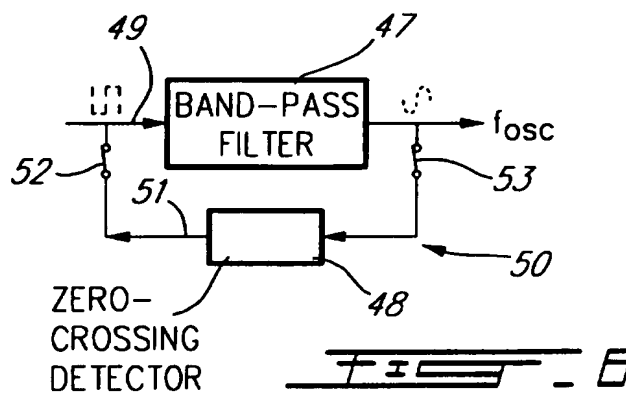
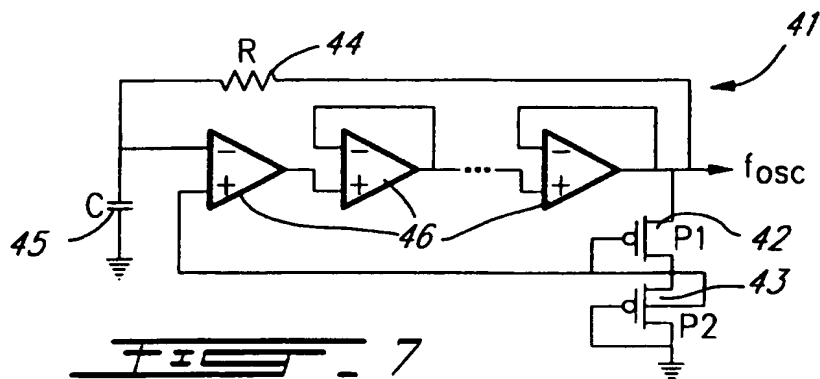
16. The device of claim 15, wherein said connecting means comprises means for successively connecting said additional circuitry to different building blocks in order to test said different buildings block with the same additional circuitry.



2/4



3/4



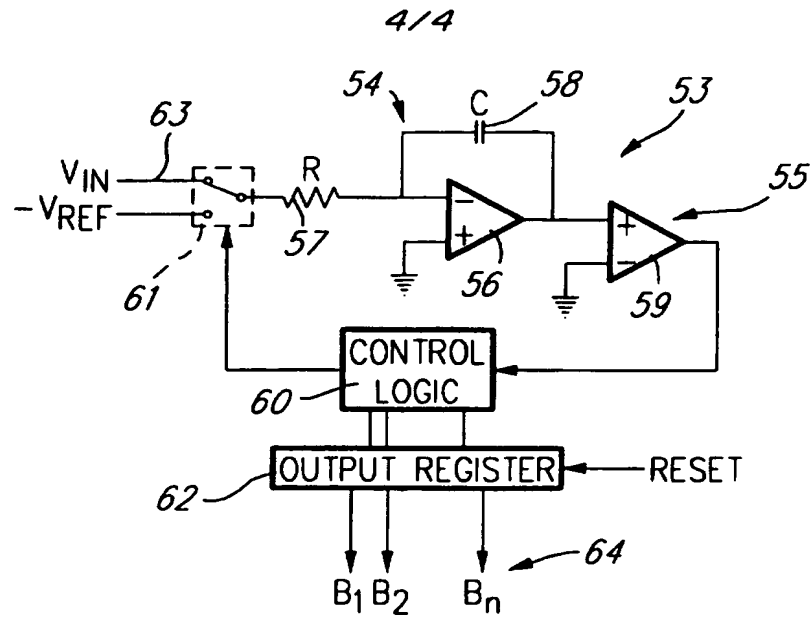


FIG. 10

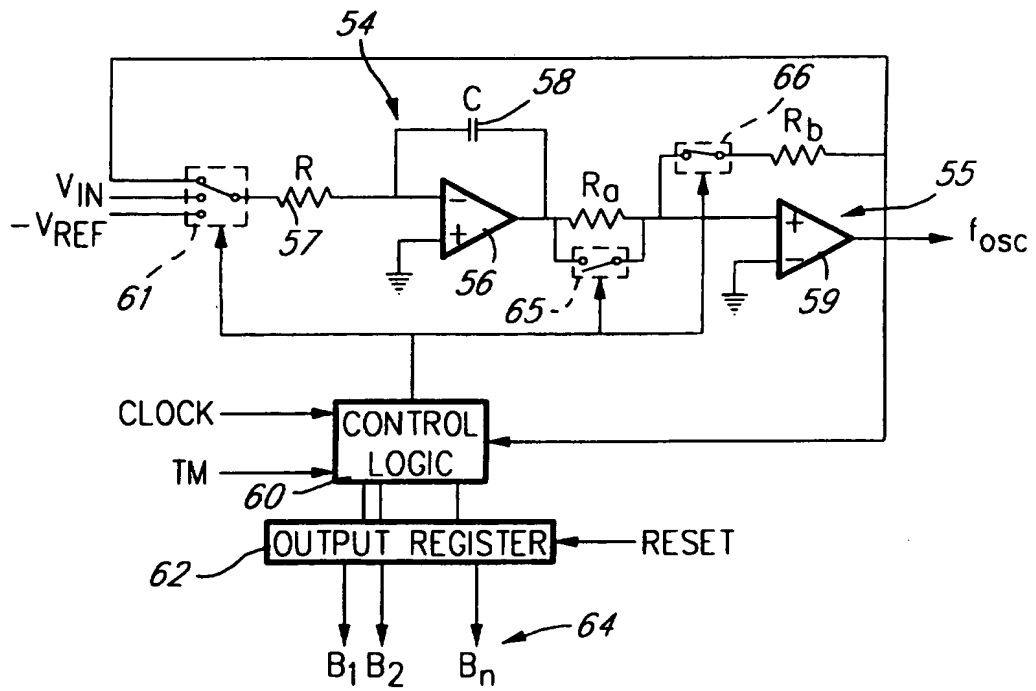


FIG. 11

INTERNATIONAL SEARCH REPORT

International Application No
PCT/CA 96/00701

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G01R31/3167 G01R31/316

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	DE,A,40 07 187 (MITSUBISHI) 20 September 1990 see claim 1	1
X	US,A,5 039 602 (MERRILL ET AL.) 13 August 1991 see column 4, line 8 - line 11	10

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents:

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- *O* document referring to an oral disclosure, use, exhibition or other means
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Date of the actual completion of the international search

2 January 1997

Date of mailing of the international search report

28. 01. 97

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/CA 96/00701

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
DE-A-4007187	20-09-90	JP-A- 2235368	18-09-90
		US-A- 5065091	12-11-91

US-A-5039602	13-08-91	US-A- 5095267	10-03-92
